REMARKS

Claims 18 and 26 have been examined with both claims rejected. Claims 29-36 have been added. Thus, claims 18, 26, and 29-36 are pending.

Claims 18 and 26

Claim 26 has been rejected under 35 USC 102(e) as being anticipated by Sokolov et al. (U.S. Patent No. 6,307,878). Also, claim 18 has been rejected under 35 USC 103(a) as being unpatentable over Sokolov in view of Krasner (U.S. Patent No. 6,272,430).

Claims 26 has been amended to recite that the searcher has a plurality of computation circuits for multi-bit correlating in a single clock cycle and in parallel the first code sequence and the second code sequence at a plurality of offsets.

Similarly, claim 18 has been amended to recite multi-bit correlating the second code sequence having the unique phase offsets with the first code sequence in each of the respective plurality of computation circuits in a single clock cycle and in parallel.

Conventional devices such as Sokolov have parallel correlators. The computing circuits 204 of the present invention support an additional level of parallel computing by performing a multi-bit correlation operation in a single clock cycle. Sokolov's correlators, on the other hand, perform one bit correlation per cycle. See Sokolov, column 5, line 6. Thus, claims 18 and 26 are patentable over the applied references for at least this reason.

Claims 29 and 30

New claims 29 and 30 recite that the memory buffer or block simultaneously receives and transmits to the computation circuits the second code sequence.

The variable memory block 216 of the present invention is used to store the received signal. Unlike the snapshot memory block 48 of Fig. 2 in Krasner, the claimed memory is not used to simply buffer data while the DSP 52 is in lower power mode. Rather, the memory block receives

the input signal and transmits multiple signal samples in parallel to the computing circuits 204 at the same time. More specifically, the memory block 216 operates in ping-pong mode, allowing one part of the memory available for computing circuits 204 and another part collecting the input signal. The memory block 216 also supports parallel memory read from multiple computing circuits 204 to multiple memory locations for performing parallel computation.

Claims 31 and 32

New claims 31 and 32 recite that the memory for the first code sequence simultaneously receives the signal and transmits multiple signal samples in parallel to each of the plurality of computation circuits. This feature is not taught in either of the applied references.

Claims 33 and 34

New claims 33 and 34 recite that wherein each of the plurality of computation circuits begins correlating simultaneously. The variable memory block 216 of the present invention collects a sufficient amount of data before the computing circuits 204 perform the computations, and then all computing circuits 204 begin correlating simultaneously. The correlators in Sokolov's scheme, on the other hand, do not start at the same time. See Sokolov, column 4, line 47.

Claims 35 and 36

New claims 35 and 36 recite that the phase of the second code sequence at each of the plurality of computation circuits is the same. Each of the correlators in Sokolov has a different code phase. See Sokolov, column 5, line 4.

Conclusion

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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